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Patent

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of Robert J. Falster
Serial No. TO BE ASSIGNED
Filed January 3, 2002
For SILICON ON INSULATOR STRUCTURE FROM LOW DEFECT DENSITY SINGLE CRYSTAL SILICON

January 3, 2002

PRELIMINARY AMENDMENT A

TO THE COMMISSIONER OF PATENTS AND TRADEMARKS,

SIR:

Please amend the application as follows:

In the Title:

Please change the title on page 1 to the following:

SILICON ON INSULATOR STRUCTURE HAVING A LOW DEFECT DENSITY DEVICE LAYER AND A PROCESS FOR THE PREPARATION THEREOF.

In the Specification:

Please replace the paragraph beginning on page 1, line 3 with the following rewritten paragraph:

CROSS-REFERENCE TO RELATED APPLICATION

This application claims priority from U.S. provisional application Serial No. 60/098,902, filed on September 2, 1998, U.S. application Serial Number 09/387,288 filed on August 31,

1999, which issued on May 22, 2001 as U.S. Patent No. 6,236,104, and U.S. application Serial Number 09/737,715 filed on December 15, 2000.

IN THE ABSTRACT:

Please replace the text in the abstract beginning on page 63, line 1 with the following rewritten text:

The present invention relates to a process for the preparation of a silicon on insulator wafer. The process includes implanting oxygen into a single crystal silicon wafer which is substantially free of agglomerated vacancy-type defects. The present invention further relates to a process for the preparation of a silicon on insulator wafer wherein oxygen is implanted into a single crystal silicon wafer having an axially symmetric region in which there is a predominant intrinsic point defect which is substantially free of agglomerated intrinsic point defects. Additionally, the present invention relates to a silicon on insulator ("SOI") structure in which the device layer and the handle wafer each have an axially symmetric region which is substantially free of agglomerated intrinsic point defects. Additionally, the present invention is directed to such a SOI structure in which the handle wafer is capable of forming an ideal, non-uniform depth distribution of oxygen precipitates upon being subjected to the heat treatment cycles of essentially any arbitrary electronic device manufacturing process.

IN THE CLAIMS

Claims 1-3 have been canceled.

New claims 4-51 have been added as follows:

4.(New) A process for the preparation of a silicon on insulator wafer, the process comprising implanting oxygen into a silicon single crystal wafer having a central axis, a circumferential edge, and a radius extending from the central axis to the circumferential edge, wherein the wafer is substantially free of agglomerated vacancy-type defects.

5.(New) The process of claim 4 wherein the silicon single crystal wafer has as oxygen content which is less than about 13 PPMA.

6.(New) The process of claim 4 wherein the silicon single crystal wafer has a concentration of carbon which is less than about $5x10^{16}$ atoms/cm^3.

7.(New) The process of claim 4 wherein the silicon single crystal wafer has a concentration of carbon which is less than about $5x10^{15}$ atoms/cm^3.

8.(New) The process of claim 4 further comprising subjecting the single crystal silicon wafer to an ideal precipitating wafer process.

9.(New) The process of claim 8 wherein the single crystal silicon wafer is subjected to the ideal precipitating wafer process prior to implanting oxygen into the wafer.

10.(New) The process of claim 8 wherein the single crystal silicon wafer is subjected to the ideal precipitating wafer process after implanting oxygen into the wafer.

11.(New) A process for the preparation of a silicon on insulator wafer, the process comprising implanting oxygen into a silicon single crystal wafer having a central axis, a circumferential edge, a radius extending from the central axis to the circumferential edge, and a first axially symmetric region in which there is a predominant intrinsic point defect which is substantially free of agglomerated intrinsic point defects.

12.(New) The process of claim 11 wherein silicon self-interstitials are the predominant intrinsic point defect within the first axially symmetric region, the first axially symmetric region extending radially inward from the circumferential edge of the wafer and having a width, as measured from the circumferential edge radially toward the central axis, which is at least about 30% of the length of the radius of the wafer.

13.(New) The process of claim 12 wherein the first axially symmetric region is generally annular in shape and the wafer additionally comprises a second axially symmetric region, that is

generally cylindrical in shape, in which vacancies are the predominant intrinsic point defect, the second region located radially inward of the first region in the wafer.

14.(New) The process of claim 11 wherein silicon self-interstitials are the predominant intrinsic point defect within the first axially symmetric region, the first axially symmetric region extending radially inward from the circumferential edge of the wafer and having a width, as measured from the circumferential edge radially toward the central axis, which is at least about 80% of the length of the radius of the wafer.

15.(New) The process of claim 14 wherein the first axially symmetric region is generally annular in shape and the wafer additionally comprises a second axially symmetric region, that is generally cylindrical in shape, in which vacancies are the predominant intrinsic point defect, the second region located radially inward of the first region in the wafer.

16.(New) The process of claim 11 wherein silicon self-interstitials are the predominant intrinsic point defect within the first axially symmetric region, the first axially symmetric region extending radially inward from the circumferential edge of the wafer and having a width, as measured from the circumferential edge radially toward the central axis, which is about equal to the length of the radius of the wafer.

17.(New) The process of claim 11 wherein the silicon single crystal wafer has as oxygen content which is less than about 13 PPMA.

18.(New) The process of claim 11 wherein the silicon single crystal wafer has a concentration of carbon which is less than about $5x10^{16}$ atoms/cm^3.

19.(New) The process of claim 11 wherein the silicon single crystal wafer has a concentration of carbon which is less than about $5x10^{15}$ atoms/cm^3.

20.(New) The process of claim 11 wherein vacancies are the predominant intrinsic point defect within the first axially symmetric region, the first axially symmetric region comprising the central axis of the wafer or having a width of at least about 15 mm, as measured along the radius of the wafer.

21.(New) The process of claim 20 further comprising a second axially symmetric region, that is generally annular in shape, in which silicon self-interstitials are the predominant intrinsic point defect, the second region being located radially outward of the first region.

22.(New) The process of claim 20 wherein the first axially symmetric region has a width which is at least about 25% of the length of the radius of the wafer.

23.(New) The process of claim 22 further comprising a second axially symmetric region, that is generally annular in shape, in which silicon self-interstitials are the predominant intrinsic point defect, the second region being located radially outward of the first region.

24.(New) The process of claim 11 wherein the first axially symmetric region has vacancies as the predominant intrinsic point defect and has a width with is about equal to the length of the radius of the wafer.

25.(New) The process of claim 11 further comprising subjecting the single crystal silicon wafer to an ideal precipitating wafer process.

26.(New) The process of claim 25 wherein the single crystal silicon wafer is subjected to an ideal precipitating wafer process prior to implanting oxygen into the wafer.

27.(New) The process of claim 25 wherein the single crystal silicon wafer is subjected to an ideal precipitating wafer process after implanting oxygen into the wafer.

28.(New) A process for the preparation of a silicon on insulator wafer, the process comprising implanting oxygen into a silicon single crystal wafer having two major, generally parallel surfaces, one of which is the front surface and the other of

which is the back surface of the silicon wafer, a central plane between the front and back surfaces, the circumferential edge joining the front and back surfaces, a surface layer which comprises a first region of the silicon wafer between the front surface and a distance, D_1, of at least about 10 micrometers, as measured from the front surface and toward the central plane, and a bulk layer which comprises a second region of the silicon wafer between the central plane and the first region, the silicon wafer having a non-uniform concentration of vacancies with the concentration of vacancies in the bulk layer being greater than the concentration of vacancies in the surface layer such that, upon subjecting the wafer to an oxygen precipitation heat treatment, a denuded zone is formed in the surface layer and oxygen clusters or precipitates are formed in the bulk layer with the concentration of the oxygen clusters or precipitates in the bulk layer being primarily dependant upon the concentration of vacancies.

29.(New) The process of claim 28 wherein D_1 is at least about 20 micrometers.

30.(New) The process of claim 28 wherein D_1 is at least about 50 micrometers.

31.(New) The process of claim 28 wherein D_1 is between about 30 and about 100 micrometers.

32.(New) The process of claim 28 wherein the wafer has a carbon concentration which is less than about 1 x 10^{16} atoms/cm^3.

33.(New) The process of claim 28 wherein the concentration of interstitial oxygen at distances greater than 3 microns from the wafer surface is at least about 50% of the concentration of interstitial oxygen in the bulk layer.

34.(New) The process of claim 28 wherein the concentration of interstitial oxygen at distances greater than 10 microns from the wafer surface is at least about 80% of the concentration of interstitial oxygen in the bulk layer.

35.(New) A process for the preparation of a silicon on insulator wafer, the process comprising implanting oxygen into a silicon single crystal wafer having two major, generally parallel surfaces, one of which is the front surface and the other of which is the back surface of the silicon wafer, a central plane between the front and back surfaces, the circumferential edge joining the front and back surfaces, a surface layer which comprises a first region of the silicon wafer between the front surface and a distance, D_1, of at least about 10 micrometers, as measured from the front surface and toward the central plane, and a bulk layer which comprises a second region of the silicon wafer between the central plane and the first region, the silicon wafer an asymmetrical vacancy concentration profile in which a maximum concentration is located between the central plane and the front

surface layer, the vacancy concentration generally increasing from the front surface to the region of maximum concentration and the difference in the concentration of vacancies in the front surface layer and the bulk layer being such that a thermal treatment at a temperature in excess of 750 °C, is capable of forming in the wafer a denuded zone in the front surface layer and oxygen clusters or precipitates in the bulk zone with the concentration of the oxygen clusters or precipitates in the bulk layer being primarily dependant upon the concentration of vacancies.

36. (New) The process of claim 35 wherein D_1 is at least about 20 micrometers.

37. (New) The process of claim 35 wherein D_1 is at least about 50 micrometers.

38. (New) The process of claim 35 wherein D_1 is between about 30 and about 100 micrometers.

39. (New) The process of claim 35 wherein the wafer has a carbon concentration which is less than about 1×10^{16} atoms/cm^3.

40. (New) The process of claim 35 wherein the concentration of interstitial oxygen at distances greater than 3 microns from the wafer surface is at least about 50% of the concentration of interstitial oxygen in the bulk layer.

41.(New) The process of claim 35 wherein the concentration of interstitial oxygen at distances greater than 10 microns from the wafer surface is at least about 80% of the concentration of interstitial oxygen in the bulk layer.

42.(New) The process of claim 35 wherein the vacancy concentration generally increases from the front surface to the region of maximum concentration and generally decreases from the region of maximum concentration to the back surface and the difference in the concentration of vacancies in the front surface layer, the back surface layer and the bulk layer being such that a thermal treatment at a temperature in excess of 750 °C, is capable of forming in the wafer a denuded zone in the front surface layer and the back surface layer and oxygen clusters or precipitates in the bulk zone with the concentration of the oxygen clusters or precipitates in the bulk layer being primarily dependant upon the concentration of vacancies.

43.(New) The process of claim 35 wherein the vacancy concentration has a first maximum concentration located in a first region of maximum concentration between the front surface layer and the central plane and a second maximum concentration located in a second region of maximum concentration between the first region of maximum concentration and the back surface layer, with the vacancy concentration generally increasing from the front surface to the first region of maximum concentration, generally decreasing from the first region of maximum

concentration to a region of minimum concentration located between the first and second maximum regions, generally increasing from the region of minimum concentration to the second region of maximum concentration and generally decreasing from the second region of maximum concentration to the back surface and the difference in the concentration of vacancies in the front surface layer, the back surface layer and the bulk layer being such that a thermal treatment at a temperature in excess of 750 °C, is capable of forming in the wafer a denuded zone in the front surface layer and in the back surface layer and oxygen clusters or precipitates in the bulk zone with the concentration of the oxygen clusters or precipitates in the bulk layer being primarily dependant upon the concentration of vacancies.

44.(New) The process of claim 43 wherein the region of minimum concentration is located between the first maximum concentration and the central plane.

45.(New) The process of claim 43 wherein the second region of maximum concentration is located at the central plane.

46.(New) The process of claim 43 wherein the vacancy concentration has a first maximum concentration located in a first region of maximum concentration between the front surface layer and the central plane and a second maximum concentration located in a second region of maximum concentration between the back surface layer and the central plane, with the vacancy

concentration generally increasing from the front surface to the first region of maximum concentration, generally decreasing from the first region of maximum concentration to the central plane, generally increasing from the central plane to the second region of maximum concentration and generally decreasing from the second region of maximum concentration to the back surface and the difference in the concentration of vacancies in the front surface layer, the back surface layer and the bulk layer being such that a thermal treatment at a temperature in excess of 750 °C, is capable of forming in the wafer a denuded zone in the front surface layer and in the back surface layer and oxygen clusters or precipitates in the bulk zone with the concentration of the oxygen clusters or precipitates in the bulk layer being primarily dependant upon the concentration of vacancies.

47.(New) A silicon on insulator structure, the structure comprising:

a single crystal silicon device layer in which there is a predominant intrinsic point defect which is substantially free of agglomerated vacancy-type defects;

a single crystal silicon handle wafer; and,

an insulating layer between the device layer and the handle wafer.

48.(New) The structure as set forth in claim 47 wherein the device layer has as oxygen content which is less than about 13 PPMA.

49.(New) The structure of claim 47 wherein the handle wafer further comprises two major, generally parallel surfaces, one of which is the front surface and the other of which is the back surface of the silicon wafer, a central plane between the front and back surfaces, the circumferential edge joining the front and back surfaces, a surface layer which comprises a first region of the silicon wafer between the front surface and a distance, D_1, of at least about 10 micrometers, as measured from the front surface and toward the central plane, and a bulk layer which comprises a second region of the silicon wafer between the central plane and the first region, the silicon wafer having a non-uniform concentration of vacancies with the concentration of vacancies in the bulk layer being greater than the concentration of vacancies in the surface layer such that, upon subjecting the wafer to an oxygen precipitation heat treatment, a denuded zone is formed in the surface layer and oxygen clusters or precipitates are formed in the bulk layer with the concentration of the oxygen clusters or precipitates in the bulk layer being primarily dependant upon the concentration of vacancies.

50.(New) The structure of claim 47 wherein the handle wafer further comprises two major, generally parallel surfaces, one of which is the front surface and the other of which is the back surface of the silicon wafer, a central plane between the front and back surfaces, the circumferential edge joining the front and back surfaces, and a denuded zone which comprises the region of the silicon wafer from the front surface to a distance, D_1, of at

least about 10 micrometers, as measured in the direction of the central plane, and which contains interstitial oxygen, the silicon wafer having a concentration of interstitial oxygen in the denuded zone at a distance equal to about one-half of D_1 is at least about 75% of the maximum concentration of interstitial oxygen in the denuded zone.

51. (New) The structure of claim 47 wherein the handle wafer further comprises two major, generally parallel surfaces, one of which is the front surface and the other of which is the back surface of the silicon wafer, a central plane between the front and back surfaces, the circumferential edge joining the front and back surfaces, a front surface layer consisting of a first region of the silicon wafer within a distance, D_2, of no more than about 15 micrometers from the front surface and a bulk layer comprising a second region of the silicon wafer between the central plane and the front surface layer, the bulk layer having a substantially uniform oxygen concentration and a concentration of crystal lattice vacancies such that upon subjecting the silicon wafer to an oxygen precipitation heat treatment consisting essentially of annealing the silicon wafer at 800°C for four hours and then at 1000°C for sixteen hours, the silicon wafer will contain oxygen precipitates having a concentration profile in which the peak density of the precipitates in the bulk layer is at or near the central plane with the concentration of the precipitates in the bulk layer generally decreasing in the direction of the front surface layer.

REMARKS

This application is a continuation application based on U.S. Application Serial No. 09/737,715 filed December 15, 2000. Support for new claims 4-51 may be found in the specification, for example, as follows:

- claims 4, 28 and 47 at page 1, line 15 through page 2, line 2 and page 35, line 25 through page 36, line 17;
- claims 5-27 and 48 at page 27, lines 4-16 and page 33, line 18 through page 34, line 19;
- claims 29-31 at page 16, line 20 through page 18 line 12;
- claim 32 at page 12, lines 11-17;
- claims 33-34 at page 18, lines 4-28;
- claims 35-46 at page 1, line 15 through page 2, line 2, page 19, line 1 through page 23 line 23 and page 35, line 25 through page 36, line 17;
- claim 49 at page 16, line 2 through page 17, line 6; and
- claims 50-51 at page 16 line 2 through page 18, line 28.

Favorable consideration and early allowance of all pending claims is requested.

* Applicant has enclosed a check in the amount of $1,412.00 to cover the fees to file this application. The Examiner is authorized to charge any underpayment or to credit any

overpayment of the above-referenced fees to Deposit Account No. 19-1345.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE TITLE:

The title has been amended as follows:

SILICON ON INSULATOR STRUCTURE **[FROM]** **HAVING A** LOW DEFECT DENSITY **[SINGLE CRYSTAL SILICON]** **HANDLE WAFER AND PROCESS FOR THE PREPARATION THEREOF**.

IN THE SPECIFICATION:

The paragraph beginning at page 1, line 3 has been amended as follows:

CROSS-REFERENCE TO RELATED APPLICATION

This application claims priority from U.S. provisional application Serial No. 60/098,902, filed on September 2, 1998 **and U.S. application Serial Number 09/387,288 filed on August 8, 1999**.

IN THE ABSTRACT:

The text of the abstract beginning on page 63, line 1 has been amended as follows:

The present invention relates to a **process for the preparation of a** silicon on insulator **[("SOI") structure having a low defect density device layer and, optionally, a handle** wafer **having improved gettering capabilities]**. The **process includes implanting oxygen into a single crystal silicon wafer** **[**device

layer comprises a central axis, a circumferential edge, a radius extending from the central axis to the circumferential edge, and a first axially symmetric region] which is substantially free of agglomerated **[intrinsic point]** **vacancy-type** defects. **The present invention further relates to a process for the preparation of a silicon on insulator wafer wherein oxygen is implanted into a single crystal silicon wafer having an axially symmetric region in which there is a predominant intrinsic point defect which is substantially free of agglomerated intrinsic point defects.** Additionally, the present invention **relates** **[is directed]** to a **silicon on insulator ("SOI")** structure **in** which **the device layer and the [has a Czochralski single crystal silicon]** handle wafer which is capable of forming an ideal, non-uniform depth distribution of oxygen precipitates upon being subjected to the heat treatment cycles of essentially any arbitrary electronic device manufacturing process.

IN THE CLAIMS:

Claims 1 through 3 have been canceled.

New Claims 4 through 59 have been added.